AIX

RISC System/6000 Model 250: The First PowerPC System

By Jim Hanna

The IBM RISC System/6000 Model 250 extends IBM's existing Model 220/230 products into the PowerPC arena. The system design achieves excellent performance at an attractive system cost with the first PowerPC processor chip, enhancing the low end of the RISC System/6000 family. This article describes some key features of the Model 250 system design.

The RISC System/6000 Model 250, the first system based on the new PowerPC technology, became available in October 1993. It maintains application binary compatibility with previous RISC System/6000 systems. The performance levels of the new processor and system design, along with the cost-effective system design based on Models 220 and 230, provide excellent price/performance in a UNIX workstation.

The key objectives of the RISC System/6000 Model 250 design include the following:

- **Software compatibility**: Minimizing the change to existing AIX RISC System/6000 system software is an important consideration. The PowerPC 601 processor chip implements most POWER Architecture instructions in addition to the 32-bit PowerPC instruction set. System-level design preserves the existing RISC System/6000 I/O model. Although simplification of the I/O structure requires changes to AIX kernel I/O services, it maintains compatibility for existing device drivers, other AIX subsystems, and—most importantly—existing applications.
- **Performance**: The 601 performance surpasses that of the previous low-end RISC System/6000 products. The PowerPC 601 processor, with its larger on-chip cache and higher operating frequency, is the major contributor to the performance improvement. System-level design provides a higher performance memory subsystem, increased bandwidth to graphics, and a higher performance I/O controller. Data moves more quickly from the processor and system memory to the graphics adapters, yielding better graphics performance.
- **Cost**: A final objective is to deliver this performance at a competitive price. The 601 processor, with its small die size, is priced very competitively. Reusing I/O components, the power supply, and the mechanical packaging originally developed for the Model 220 allows existing Model 220/230 systems to be upgraded to the PowerPC. This reduces overall costs and lowers the price of new systems.

System Overview

Good performance at a reasonable cost was the design goal of the Model 250 system structure. The processor and optional graphics subsystem attach directly to system memory with a multi-master system bus. A high-performance Micro Channel® bridge chip attaches the I/O subsystem to the system bus. The following sections detail each component shown in Figure 1.

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The Model 250

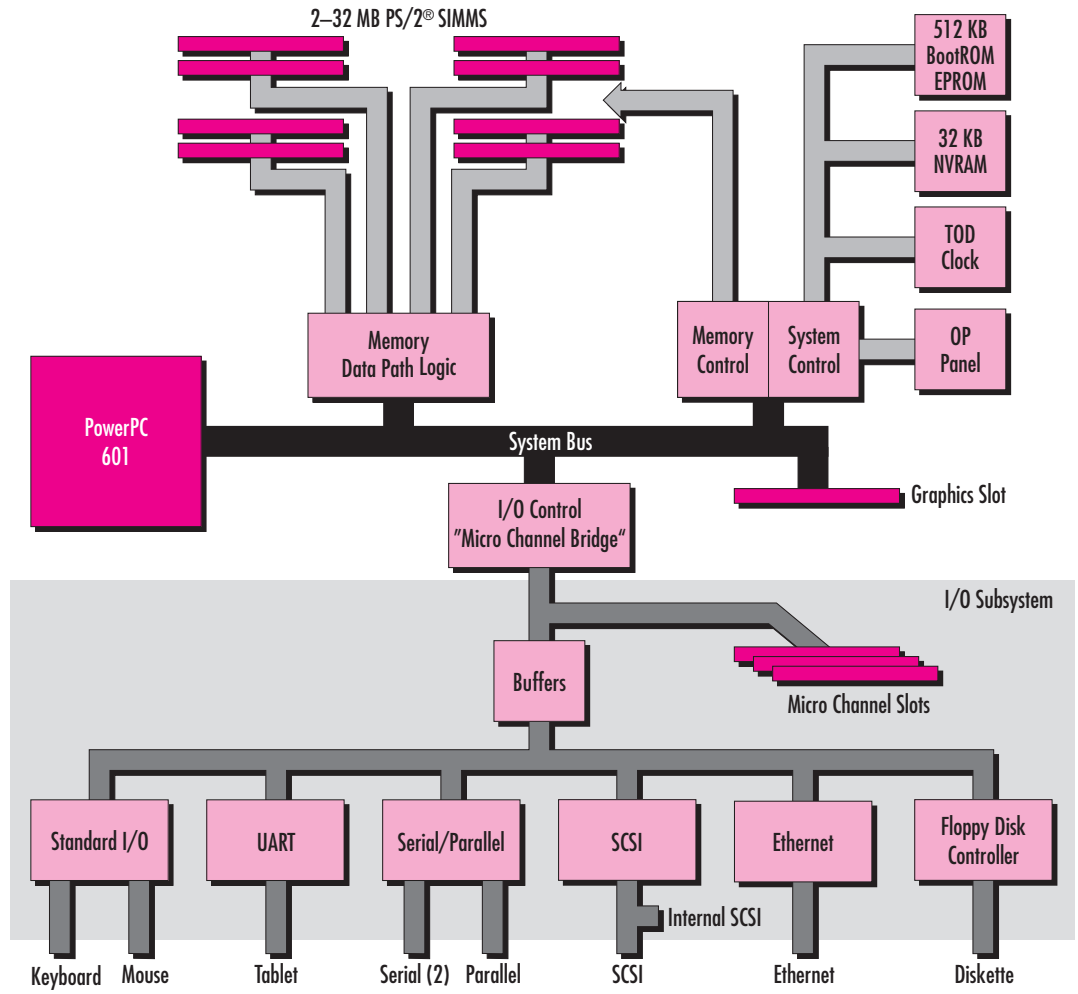

Figure 1. The Model 250

PowerPC 601 Processor

The article "PowerPC 601 Microprocessor" in this issue describes the PowerPC 601 processor chip. There are several notable features influencing the Model 250 system design. The 601 chip uses a Motorola 88110-based processor interface that extends into the low-cost, high-performance Model 250 system bus. The system design exploits the ability of the 601 to operate its interface more slowly than the base processor frequency; the Model 250 runs the 601 at 66 MHz and the system bus at 33 MHz. By including a large, 32 KB, eight-way set-associative cache, a system can achieve competitive performance without an expensive second-level cache. The low power consumption of the 601 chip allows the Model 250 to use the power supply and mechanical packaging previously designed for Models 220 and 230.

System Bus

The Model 250 system bus is an extension of the PowerPC processor interface, which in turn is a derivative of the Motorola 88110 interface. The system bus is synchronous and has an 8-byte bidirectional data bus and an independent 32-bit address bus. In addition to the basic processor functions of memory load/store and Programmed

I/O (PIO) load/store, the Model 250 system bus supports interrupt routing, byte steering for 4-byte devices, and protocols for system configuration. The system maintains memory coherency with a four-state snooping protocol.

The system bus operates at 33 MHz in the Model 250. Single-level pipelining is implemented, allowing a second bus address to be placed on the bus before the data phase of the first bus transaction is completed. This yields four 8-byte data transfers every five bus clocks, for a maximum system bus bandwidth of 213 MB per second.

The address and data buses have byte parity to ensure data integrity. The bus provides a data retry function to allow stored data to be forwarded simultaneously with checking the Error Correcting Code (ECC).

Memory

The RISC System/6000 Model 250 can support system memory capacities from 16 MB to 256 MB. As in previous RISC System/6000 Models 220, 230, and M20, standard 36-bit DRAM Single In-line Memory Modules (SIMMs) from the personal computer industry minimize cost. The Model 250 can use the 2 MB PS/2-style SIMMs, as well as the 4 MB and 8 MB PS/2 SIMMs that were used in earlier models. In addition, the system can use the new JEDEC standard 16 MB and 32 MB SIMMs. The maximum capacity of the Model 250 is eight SIMMs.

Interleaving provides sufficient memory subsystem performance from standard 70 nanosecond DRAMs. The memory system implements two banks of two SIMMs each, requiring installation of SIMMs in matched sets of four. The memory controller supports the cache sector fill/flush characteristics of the 601 processor using a 32-byte load/store buffer. These features yield a memory bandwidth of 142 MB per second for loads and 213 MB per second for stores.

The memory subsystem implements ECC; the system corrects single-bit errors "on the fly" for loads from memory by using the data retry capability of the system bus. Double-bit errors cause a machine check to preserve data integrity. Since the memory maintains ECC codes on 8-byte double-words, the DRAM cost penalty is the same as byte parity. The memory subsystem performs read-modify-write operations to enable stores of less than 8 bytes.

System Control

The Model 250 implements system control functions, such as the system bus arbiter and the system interrupt controller, in the same Application Specific Integrated Circuit (ASIC) that contains the memory control logic.

The system bus requires a centralized arbiter that delegates bus resources to contending devices and controls pipelining. It manages the various system bus functions such as interrupt transactions, extended (PIO) cycles, and snooping in a way that promotes efficient use of the system bus.

The system interrupt controller design enables interrupt requests to be routed over the system bus. The controller fields interrupt request transactions from devices attached to the system bus. Depending on the current operating priority of the processor, the interrupt controller either activates the processor's interrupt signal or generates an interrupt reset bus transaction and conveys it back to the interrupting device. The controller instructs the device to retry the request later. The interrupt controller also sends a reset transaction to the interrupting device when the processor successfully completes the interrupt.

BootROM

The BootROM on the Model 250 is based on the Model 220/230 design. It was necessary to modify the Power-On Self Test (POST) to accommodate the 601 processor and new system ASICs. The POST tests all system elements required to load the operating system boot image into system memory. These elements include the processor, system memory, I/O controller, and any I/O device required for the boot process, including network devices. The system passes the results of this testing and configuration activity to the operating system through the enhanced IPL Control Block in main memory or sends the results to the Operator Panel LED display to assist in diagnosing the system.

After the system is verified and configured, the operating-system boot image is loaded into system memory. Sufficient device driver capability to transfer the boot image from media to system memory can be included in the BootROM firmware itself. It can also be included in ROM located on I/O devices that can be accessed with a ROM scan technique. Boot lists maintained in NVRAM are used for selecting boot devices. The position of the Operator Panel key switch determines which boot list to follow. The selected boot list organizes the boot images from multiple devices

AIX POWER Solutions Catalog

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in order of importance. Menus allow the user to enter network parameters necessary for booting over certain types of networks.

Graphics

The 2-D graphics adapter developed for the Model 250 provides 8-bit color graphics with both 1024 x 768 and 1280 x 1024 resolutions. The Model 250 continues the Model 220/230 strategy of attaching low-cost graphics to a high-performance, low-latency local bus. The Model 250 improves on the Model 220/230 design by attaching a graphics card directly to the system bus, which provides higher performance levels than the local I/O buses used previously, and by using a more powerful, single-chip rasterizer. This combination promotes excellent X-Windows performance of about 1.6 million X11 2-D vectors per second.

I/O Subsystem

As with earlier RISC System/6000 products, the Micro Channel I/O bus is the basis of the I/O subsystem. The Model 250 supports two Micro Channel slots. By simplifying the RISC System/6000 I/O architecture for PowerPC systems, IBM reduced hardware costs. Hardware-enforced coherency is used instead of the AIX-managed coherency of previous RISC System/6000 products, simplifying I/O software. The system retains the recovery capabilities of the RISC System/6000 I/O architecture.

A new I/O control ASIC bridges the Micro Channel bus and the system bus. It contains the Micro Channel bus arbiter, Direct Memory Access (DMA) controller, interrupt controller, and configuration support. Extended protocol transactions on the system bus allow for PIO to the Micro Channel. A 64-byte PIO buffer helps PIO performance. Micro Channel bus masters access system memory through the I/O control ASIC, which acts as a memory slave. A 64-byte bus-master cache and a 32-byte DMA slave buffer provide high-performance access to system bus-attached memory. The Model 250 supports an 8-byte 10 MHz streaming data protocol that has a peak data rate of 80 MB per second.

The Model 250 provides the standard complement of RISC System/6000 integrated I/O devices: a keyboard, mouse, tablet, parallel port, and two serial ports. The integrated Ethernet function is improved over previous models by including twisted-pair media (10BaseT) capability as well as thick (10Base5). The integrated Small Computer Systems Interface (SCSI) function is improved with the addition of 10 MB per second "fast" SCSI capability.

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